The collaboration research for the Dual Graduate School between VNU and JAIST

[Title of collaboration research]:

Study on electrical defect of Si near the interface with low-temperature SiO_2 film on nano-scale

[The members of collaboration research]:

1

[Reference home-page]: http://www.jaist.ac.jp/ms/labs/handoutai/horita-lab/ Paper1.pdf

[Other references]: P. N. Hai, K. Nishio and S. Horita, "Silicon oxide formation for TFTs using humid ozone-enriched gas ambient at low temperature",Proc. 34th European Solid-State Device Research Conference, Leuven, Belgium, pp.313-316, 21-23 Sept. 2004.

[Contents]

Low-temperature polycrystalline silicon thin film transistor (LT poly-Si TFT) is a key device in active-matrix liquid-crystal displays (AM-LCD) fabricated on glass substrates which is non-heat resistant. The device performance is governed by the quality of the gate insulator as well as that of the device body of the Si film. Therefore, the formation method of device-quality gate oxide at lower temperature below 400°C is desired for high-performance LT poly-Si TFTs. Although, for low temperature fabrication, they generally use the deposition method with plasma, it has a serious problem to cause plasma damage to fabricated devices. For this requirement, we have reported an effective and low-cost deposition method of silicon oxide film in which O_3 gas (1%) and the silicone oil vapor generated by bubbling the silicone oil with N_2 gas are mixed and heated to react each other at the temperature lower than 250°C as shown Fig. 1. In spite of low temperature deposition process, the film quality is as good as that of the plasma enhanced chemical vapor deposition (PECVD) method at the temperature of 350°C. However, the property of the interface between the Si and the deposited Si oxide film is not so good and should be more improved up to commercial level. One of the interface problems is deep energy level in the band gap of the Si. In the low-temperature-deposited Si oxide film, the OH impurities are contained and they react with Si at the interface in nano-scale during the deposition. Then, the interface of Si is imperfectly oxidized and some defects are generated in nano-scale. These defects are the source of deep energy level in the band gap.

So, in this research, the Vietnam side characterizes the nano-scale interface electrical defect in the Si substrate by using deep level transition spectroscopy (DLTS) measurement system. Taking the evaluation result into account, our JAIST side tries to improve the quality of the Si oxide film, e. g., reduce the amount of OH impurity in the deposited film, by adjusting the deposition condition.

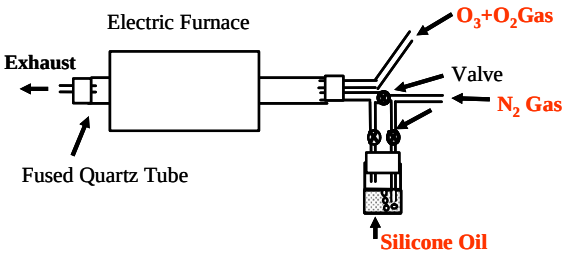

Fig. 1. Si oxide film deposition system using silicone oil and ozone gas.

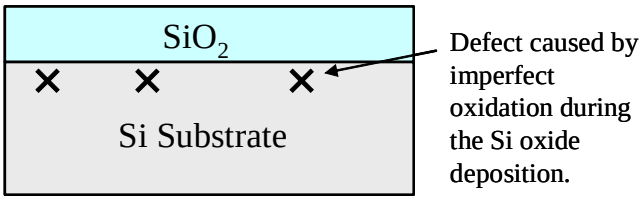

Fig. 2. Schematic drawing of defect generation near the interface of Si in nano-scale.